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DATA REWRITE CONTROL IN DATA  
TRANSFER & STORAGE APPARATUS (30010360)  
JORGE ANTONIO SVED

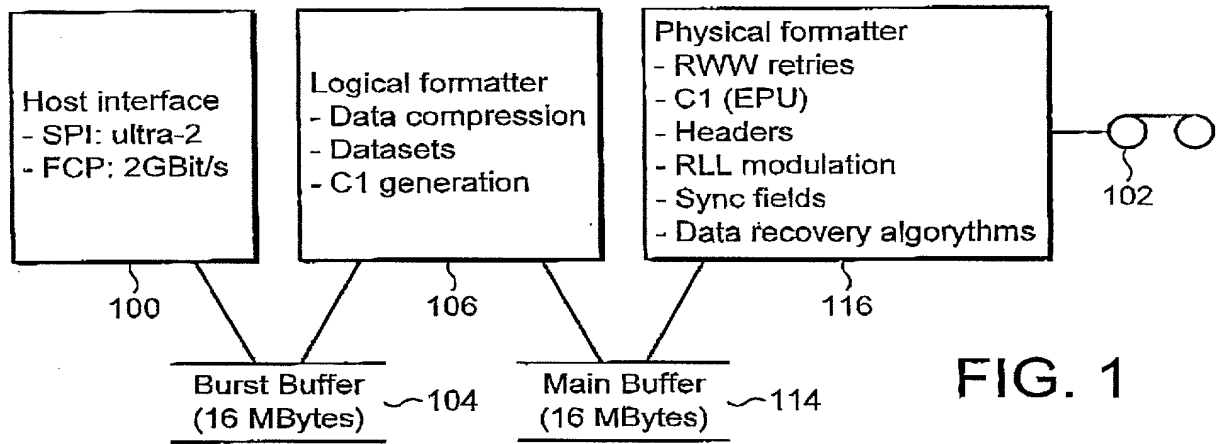


FIG. 1

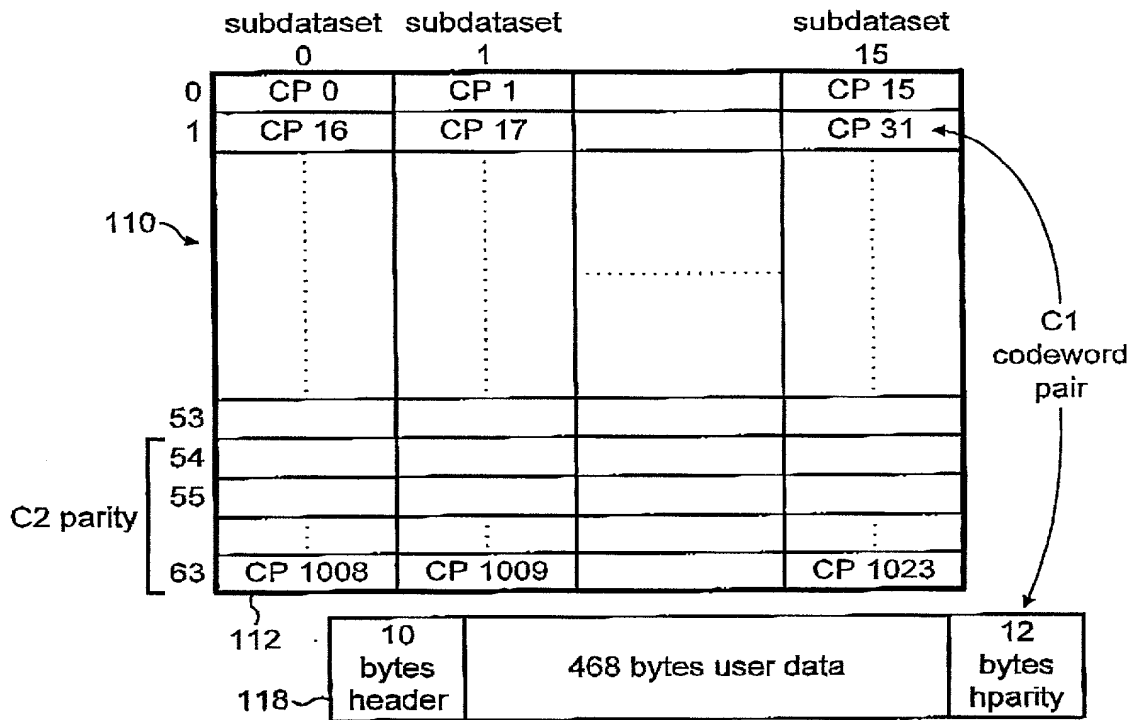


FIG. 2

# DATA REWRITE CONTROL IN DATA TRANSFER & STORAGE APPARATUS (30010360)

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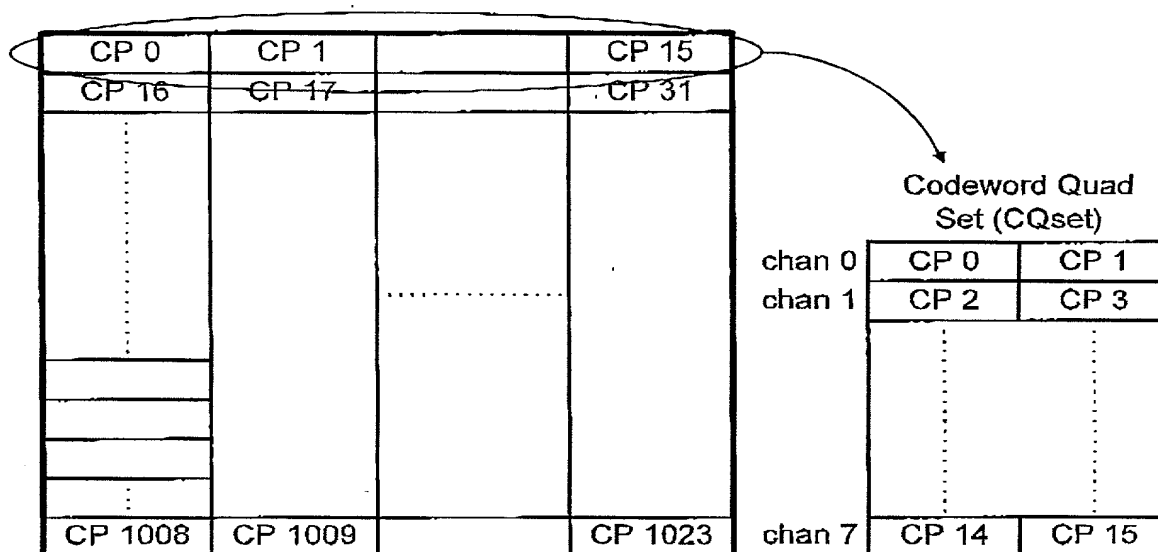


FIG. 3

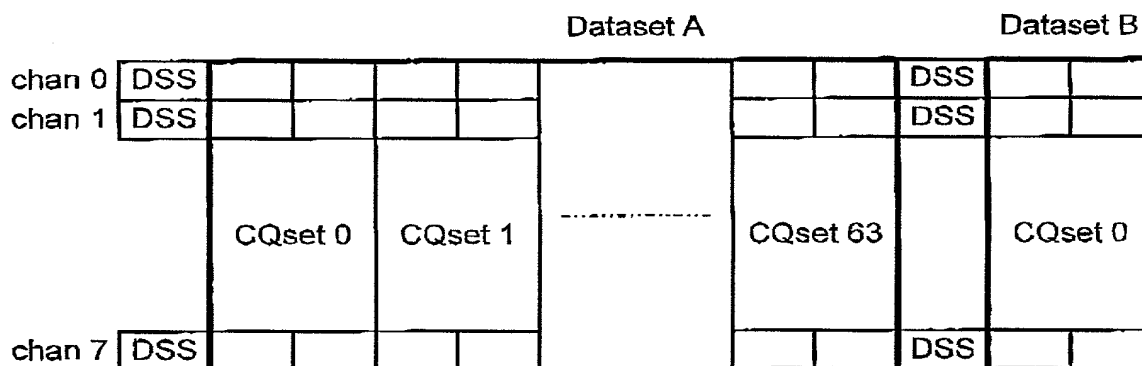


FIG. 4

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a	b	c	d	e	f
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FIG. 5

Trk	W	0	0	0	1	1	1	2	2	2	2	3	3	3	3
N	0 <sup>x</sup>	1	2	0 <sup>x</sup>	3 <sup>x</sup>	4	0"	3 <sup>x</sup>	5	6	3"	7	8	9	
0	D S S	0	9	18	1'	27	36	2"	29'	45	54	30"	63	64	27
1		1	10	19	2'	28	37	3"	30'	46	55	31"	56	65	74
2		2	11	20	3'	29	38	4"	31'	47	48	24"	57	66	75
3		3	12	21	4'	30	39	5"	24'	40	49	25"	58	67	76
4		4	13	22	5'	31	32	6"	25'	41	50	26"	59	68	77
5		5	14	23	6'	24	33	7"	26'	42	51	27"	60	69	78
6		6	15	16	7'	25	34	0"	27'	43	52	28"	61	70	79
7		7	8	17	0'	26	35	1"	28'	44	53	29"	62	71	72

FIG. 6

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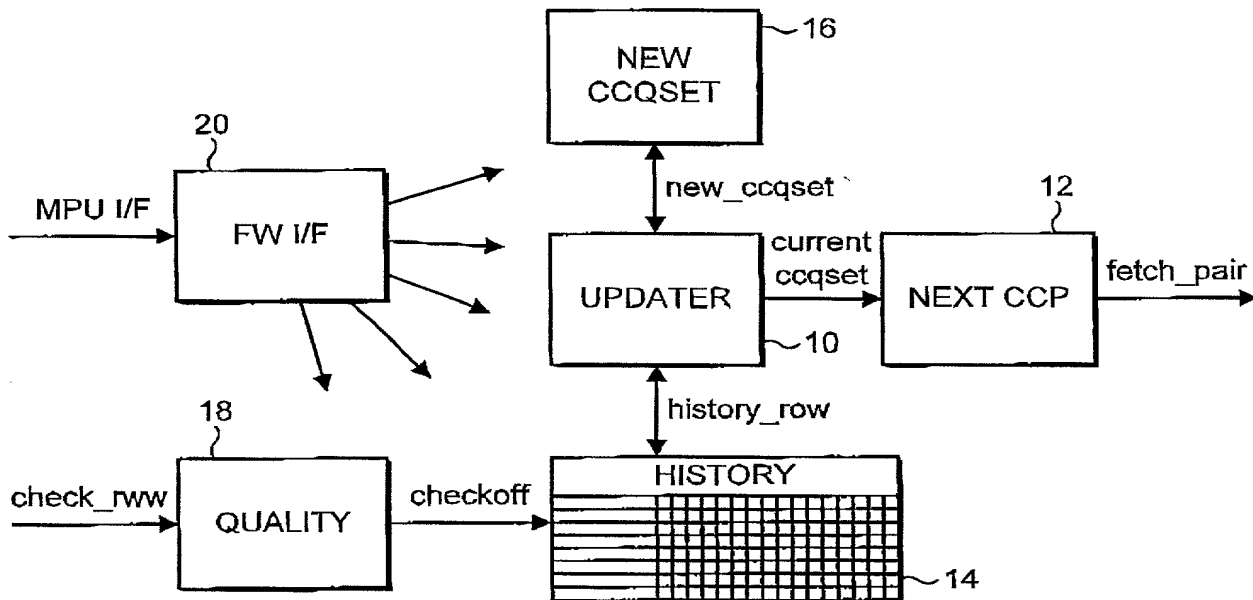


FIG. 7

Bit name	Bit	Description
go	0	1=>Enables the whole WCC Function
	2:1	Unused now. Used to be <i>channels</i> and <i>odd_tracks</i>
reserved_bit	3	Header reserved bit (programme a 0 here)
strict_rewrites	4	1=>CCQ Set always rewritten unless all its CCQs are good regardless of previous rewrites
latency (2:0)	7:5	Latency is the rewrite distance in intervening CCQ Sets between instances of the same CCQ Set
no_new_dataset	8	Write 0 here. (1 is only used for HW debug)

FIG. 8